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ORIGINAL ARTICLE

Selection of DC voltage magnitude using Fibonacci series for new hybrid asymmetrical multilevel inverter with minimum PIV

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KEYWORDS

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PIV

Abstract Multilevel inverters are suggested to obtain high quality output voltage. In this paper, a new hybrid configuration is proposed, obtained by cascading one four switches H-bridge cell with a family of multilevel inverters. In addition, by the use of specific sequence for value of DC sources named Fibonacci series, asymmetrical topology of proposed inverter is introduced. Main advantages are that proposed inverter has least Peak Inverse Voltage (PIV) than other conventional multilevel converters in both symmetric and asymmetric modes. Also, this topology doubles the number of output levels using only one cascaded four switches H-bridge cell. The PCI-1716 DAQ using PC has been used to generate switching pulses in experimental results. For presenting valid performance of proposed configuration, simulation results carried out by MATLAB/SIMULINK software and the validity of the proposed multilevel inverter is verified by experimental results.

1. Introduction

High-power industrial applications of converters have been revolutionized in the recent decades by the advent of multilevel converters [1]. Lately, multilevel converters have presented an important development to reach higher power with increasing voltage levels [2]. Also many multilevel inverter configurations and pulse width modulation (PWM) techniques are presented to improve the output voltage harmonic spectrum [3–5]. Multilevel inverters can be considered as voltage synthesizers, wherein the output voltage is synthesized from many discrete smaller voltage levels. Compared with the traditional two-level voltage inverter, the main advantages of the multilevel inverters are having smaller output voltage step, lower harmonic components, better electromagnetic compatibility and lower switching losses [2,6–9]. They can also operate at both fundamental switching frequency and higher switching frequencies in accord with the implementations [9]. But, the main drawbacks of the multilevel inverters are the use of a larger number of semiconductors and a complex control circuitry and needing the balancing of the voltage at the boundaries of capacitors [10,11].

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From among voltage source multilevel converters, cascaded and modular multilevel converters offer several benefits such as possibility of eliminating ac side filters and interfacing transformer in some applications where it is appropriate, low dv/dt and switching losses as converter switches operate at low frequency [12,13].

In the present paper, a new hybrid symmetric and hybrid asymmetric topology of multilevel inverter has been investigated. In symmetrical mode the value of PIV and the number of switches versus other conventional symmetric converters has been reduced. For magnitude selection of DC voltage sources in asymmetrical mode Fibonacci series [14], has been used. This cause significant reduction in total switches PIV with respect to other multilevel topologies. Simulation results and comparison studies and experimental results verify validity of theoretical consideration.

2. Case study

2.1. Conventional cascaded H-bridge multilevel inverter

One of the basic structures for multilevel inverters is cascaded H-bridge inverter. Fig. 1 shows a single phase cascaded multilevel inverter.

In cascaded H-bridge multilevel inverters each DC source is connected to different stages. If all DC voltage sources in Fig. 1, equal to $V_{dc} = 1pu$, the converter is known as symmetric multilevel inverter. In symmetric topology, each cell can generate three voltage levels $+V_{dc}$, 0, $-V_{dc}$. The number of output voltage levels can be obtained by:

$$m = 2n + 1 \tag{1}$$

and PIV is given by:

$$PIV = 4nV_{dc} \tag{2}$$

where n is the number of DC sources and m is the number of voltage levels. To obtain large number of output voltage levels, asymmetric multilevel inverter can be used. In binary topology of asymmetric cascaded multilevel inverter, maximum output voltage levels and PIV are given by:

$$m = 2^{n+1} - 1 \quad \text{if} \quad V_{dci} = 2^{i-1}V_{dc} \quad \text{for} \quad i = 1, 2, \ldots, n \tag{3}$$

$$PIV = 4(2^n - 1)V_{dc} \tag{4}$$

and in trinary topology, maximum output voltage levels and PIV are given by:

$$m = 3^n \quad \text{if} \quad V_{dci} = 3^{i-1}V_{dc} \quad \text{for} \quad i = 1, 2, \ldots, n \tag{5}$$

$$PIV = 2(3^n - 1)V_{dc} \tag{6}$$

2.2. A symmetrical topology of multilevel inverter

In [15], a new symmetrical topology of multilevel inverter is introduced, as presented in Fig. 2. In this configuration all of negative and positive levels can be obtained.

This configuration consists of DC voltage sources and $(2n + 2)$ unidirectional switches. Maximum output voltage can be obtained as follows:

$$V_{O_{max}} = V_1 + V_2 + \ldots + V_n, \qquad V_1 = V_2 = \ldots = V_n \tag{7}$$

For $V_n = V_{dc}$, maximum output voltage will be $V_{O_{max}} = nV_{dc}$. The number of output voltage levels and PIV can be obtained by:

$$m = 2n + 1 \tag{8}$$

$$PIV = 4nV_{dc} \tag{9}$$

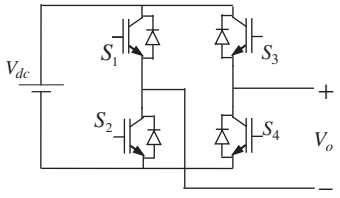

Figure 3 Four switches three level H-bridge inverter.

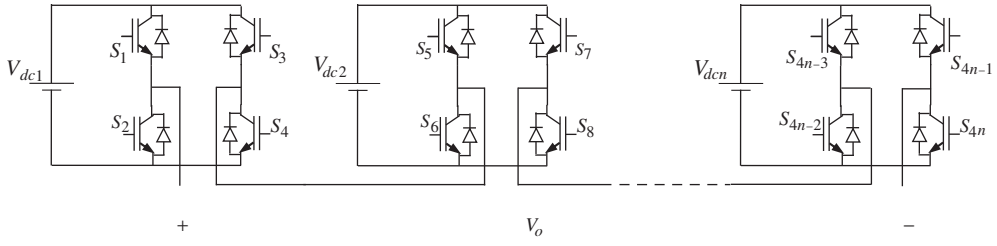

Figure 1 Single phase cascaded multilevel inverter.

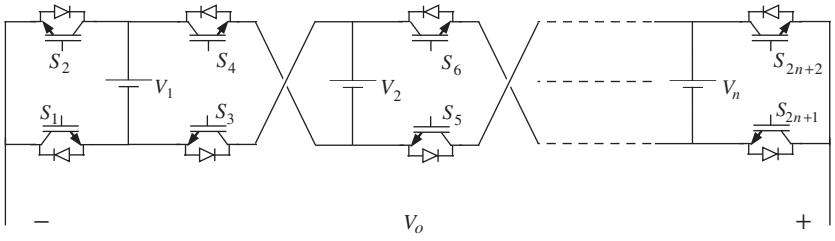

Figure 2 Family of multilevel inverters proposed in [15].

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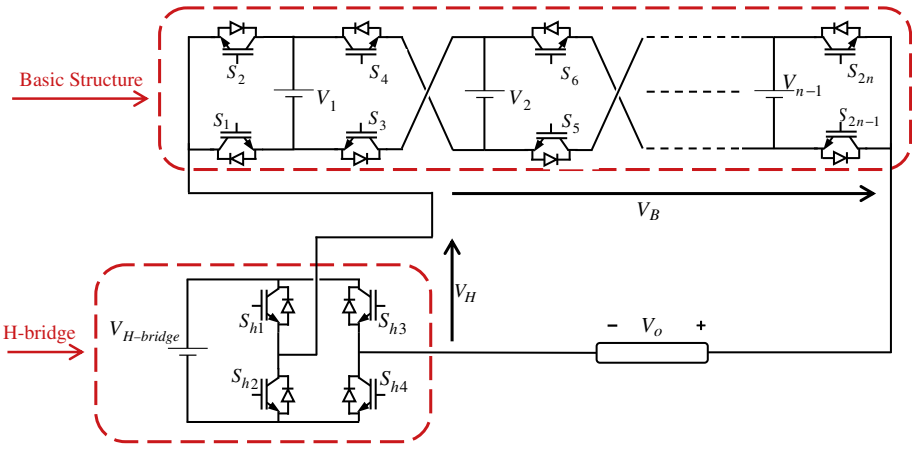

Figure 4 Proposed structure.

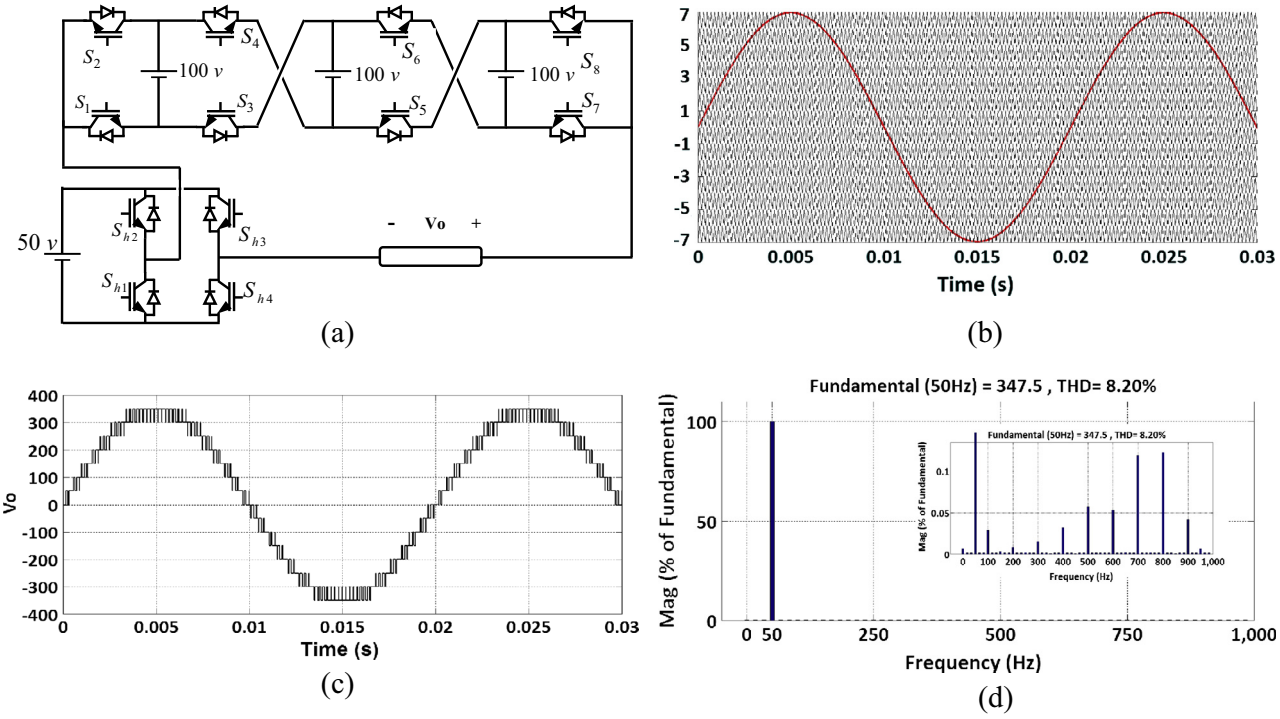

Figure 5 Operation of 15-level proposed symmetric converter: (a) The configuration of a 15-level proposed symmetric MLI; (b) Carriers and reference signals; (c) Output voltage; (d) Frequency spectrum of output voltage.

3. Proposed topology

3.1. Hybrid symmetric converter

In this paper, to increase the output voltage levels only four switches H-bridge inverter in Fig. 3 has been mixed by specific topology shown in Fig. 2 as series (Fig. 4).

In proposed converter, with n DC sources, in order to double the number of output voltage levels in specific configuration basic structure, H-bridge DC source value is selected half of the minimum value of basic structure DC voltage sources. For example, if all DC voltage sources in Fig. 4 are equal to $V_{dc} = 1pu$, selected value for H-bridge DC source will be $\frac{1}{2}V_{dc} = 0.5pu$.

In Fig. 4 value of $V_{H-bridge}$ is $\frac{V_{i(\min)}}{2} = \frac{V_1}{2}$. Since in hybrid symmetric topology, DC voltage sources in basic structure are the same, this inverter can be known as a symmetric multilevel inverter. The number of output voltage levels, is obtained by $m = 4n - 1$, where n is the number of DC voltage sources.

The PIV value of hybrid symmetric topology is given by:

$$PIV = (4n - 2)V_{dc} \tag{10}$$

Table 1 ON state switches lookup table for symmetric proposed topology.

Output voltage	ON state switches
+350	(S_1, S_4, S_6, S_8, S_{h2}, S_{h4})
+300	(S_1, S_4, S_6, S_8, S_{h2}, S_{h3}) or (S_1, S_4, S_6, S_8, S_{h1}, S_{h4})
+250	(S_1, S_4, S_6, S_8, S_{h1}, S_{h3}) or (S_2, S_4, S_6, S_8, S_{h2}, S_{h4}) (S_1, S_4, S_6, S_7, S_{h2}, S_{h4})
+200	(S_2, S_4, S_6, S_8, S_{h2}, S_{h3}) or (S_2, S_4, S_6, S_8, S_{h1}, S_{h4}) (S_1, S_4, S_6, S_7, S_{h2}, S_{h3}) or (S_1, S_4, S_6, S_7, S_{h1}, S_{h4})
+150	(S_2, S_4, S_6, S_8, S_{h1}, S_{h3}) or (S_1, S_4, S_6, S_7, S_{h1}, S_{h3}) (S_1, S_3, S_6, S_8, S_{h2}, S_{h4}) or (S_2, S_4, S_6, S_7, S_{h2}, S_{h4}) (S_1, S_4, S_5, S_8, S_{h2}, S_{h4})
+100	(S_1, S_3, S_6, S_8, S_{h2}, S_{h3}) or (S_1, S_3, S_6, S_8, S_{h1}, S_{h4}) (S_2, S_4, S_6, S_7, S_{h2}, S_{h3}) or (S_2, S_4, S_6, S_7, S_{h1}, S_{h4}) (S_1, S_4, S_5, S_8, S_{h2}, S_{h3}) or (S_1, S_4, S_5, S_8, S_{h1}, S_{h4})
+50	(S_1, S_3, S_6, S_8, S_{h1}, S_{h3}) or (S_2, S_4, S_6, S_7, S_{h1}, S_{h3}) (S_1, S_4, S_5, S_8, S_{h1}, S_{h3}) or (S_2, S_4, S_5, S_8, S_{h2}, S_{h4}) (S_1, S_3, S_6, S_7, S_{h2}, S_{h4}) or (S_2, S_3, S_6, S_8, S_{h2}, S_{h4}) (S_1, S_4, S_5, S_7, S_{h2}, S_{h4})
0	(S_2, S_4, S_5, S_8, S_{h2}, S_{h3}) or (S_2, S_4, S_5, S_8, S_{h1}, S_{h4}) (S_2, S_3, S_6, S_8, S_{h2}, S_{h3}) or (S_2, S_3, S_6, S_8, S_{h1}, S_{h4}) (S_1, S_4, S_5, S_7, S_{h2}, S_{h3}) or (S_1, S_4, S_5, S_7, S_{h1}, S_{h4})
−50	(S_2, S_4, S_5, S_7, S_{h2}, S_{h4}) or (S_1, S_3, S_5, S_8, S_{h2}, S_{h4}) (S_2, S_3, S_6, S_7, S_{h2}, S_{h4}) or (S_2, S_4, S_5, S_8, S_{h1}, S_{h3}) (S_1, S_3, S_6, S_7, S_{h1}, S_{h3}) or (S_2, S_3, S_6, S_8, S_{h1}, S_{h3}) (S_1, S_4, S_5, S_7, S_{h1}, S_{h3})
−100	(S_2, S_4, S_5, S_7, S_{h2}, S_{h3}) or (S_2, S_4, S_5, S_7, S_{h1}, S_{h4}) (S_1, S_3, S_5, S_8, S_{h2}, S_{h3}) or (S_1, S_3, S_5, S_8, S_{h1}, S_{h4}) (S_2, S_3, S_6, S_7, S_{h2}, S_{h3}) or (S_2, S_3, S_6, S_7, S_{h1}, S_{h4})
−150	(S_1, S_3, S_5, S_7, S_{h2}, S_{h4}) or (S_2, S_3, S_5, S_8, S_{h2}, S_{h4}) (S_2, S_4, S_5, S_7, S_{h1}, S_{h3}) or (S_1, S_3, S_5, S_8, S_{h1}, S_{h3}) (S_2, S_3, S_6, S_7, S_{h1}, S_{h3})
−200	(S_1, S_3, S_5, S_7, S_{h2}, S_{h3}) or (S_1, S_3, S_5, S_7, S_{h1}, S_{h4}) (S_2, S_3, S_5, S_8, S_{h2}, S_{h3}) or (S_2, S_3, S_5, S_8, S_{h1}, S_{h4})
−250	(S_2, S_3, S_5, S_7, S_{h2}, S_{h4}) or (S_1, S_3, S_5, S_7, S_{h1}, S_{h3}) (S_2, S_3, S_5, S_8, S_{h1}, S_{h3})
−300	(S_2, S_3, S_5, S_7, S_{h2}, S_{h3}) or (S_2, S_3, S_5, S_7, S_{h1}, S_{h4})
−350	(S_2, S_3, S_5, S_7, S_{h1}, S_{h3})

Table 2 ON state switches lookup table for asymmetric proposed topology.

Output voltage	ON state switches
+450	(S_1, S_4, S_6, S_8, S_{h2}, S_{h4})
+400	(S_1, S_4, S_6, S_8, S_{h1}, S_{h3}) or (S_1, S_4, S_6, S_8, S_{h1}, S_{h4})
+350	(S_1, S_4, S_6, S_8, S_{h2}, S_{h3}) or (S_2, S_4, S_6, S_8, S_{h1}, S_{h4})
+300	(S_2, S_4, S_6, S_8, S_{h2}, S_{h3}) or (S_2, S_4, S_6, S_8, S_{h1}, S_{h4})
+250	(S_2, S_4, S_6, S_8, S_{h1}, S_{h3}) or (S_1, S_3, S_6, S_8, S_{h2}, S_{h4}) (S_1, S_4, S_6, S_7, S_{h2}, S_{h4})
+200	(S_1, S_3, S_6, S_8, S_{h2}, S_{h3}) or (S_1, S_3, S_6, S_8, S_{h1}, S_{h4}) (S_1, S_4, S_6, S_7, S_{h2}, S_{h3}) or (S_1, S_4, S_6, S_7, S_{h1}, S_{h4})
+150	(S_1, S_3, S_6, S_8, S_{h1}, S_{h3}) or (S_1, S_4, S_6, S_7, S_{h1}, S_{h3}) (S_2, S_3, S_6, S_8, S_{h1}, S_{h4}) or (S_2, S_4, S_6, S_7, S_{h2}, S_{h4}) (S_1, S_4, S_5, S_8, S_{h2}, S_{h4})
+100	(S_2, S_3, S_6, S_8, S_{h2}, S_{h3}) or (S_2, S_3, S_6, S_8, S_{h1}, S_{h4}) (S_2, S_4, S_6, S_7, S_{h2}, S_{h3}) or (S_2, S_4, S_6, S_7, S_{h1}, S_{h4}) (S_1, S_4, S_5, S_8, S_{h2}, S_{h3}) or (S_1, S_4, S_5, S_8, S_{h1}, S_{h4})
+50	(S_2, S_3, S_6, S_8, S_{h1}, S_{h3}) or (S_2, S_4, S_6, S_7, S_{h1}, S_{h3}) (S_1, S_4, S_5, S_8, S_{h1}, S_{h3}) or (S_2, S_4, S_5, S_8, S_{h2}, S_{h4}) (S_1, S_3, S_6, S_7, S_{h2}, S_{h4})
0	(S_2, S_4, S_5, S_8, S_{h2}, S_{h3}) or (S_2, S_4, S_5, S_8, S_{h1}, S_{h4}) (S_1, S_3, S_6, S_7, S_{h2}, S_{h3}) or (S_1, S_3, S_6, S_7, S_{h1}, S_{h4})
−50	(S_1, S_4, S_5, S_7, S_{h2}, S_{h4}) or (S_1, S_3, S_5, S_8, S_{h2}, S_{h4}) (S_2, S_3, S_6, S_7, S_{h2}, S_{h4}) or (S_2, S_4, S_5, S_8, S_{h1}, S_{h3}) (S_1, S_3, S_6, S_7, S_{h1}, S_{h3})
−100	(S_1, S_4, S_5, S_7, S_{h2}, S_{h3}) or (S_1, S_4, S_5, S_7, S_{h1}, S_{h4}) (S_1, S_3, S_5, S_8, S_{h2}, S_{h3}) or (S_1, S_3, S_5, S_8, S_{h1}, S_{h4}) (S_2, S_3, S_6, S_7, S_{h2}, S_{h3}) or (S_2, S_3, S_6, S_7, S_{h1}, S_{h4})
−150	(S_2, S_4, S_5, S_7, S_{h2}, S_{h4}) or (S_2, S_3, S_5, S_8, S_{h2}, S_{h4}) (S_1, S_4, S_5, S_7, S_{h1}, S_{h3}) or (S_1, S_3, S_5, S_8, S_{h1}, S_{h3}) (S_2, S_3, S_6, S_7, S_{h1}, S_{h3})
−200	(S_2, S_4, S_5, S_7, S_{h2}, S_{h3}) or (S_2, S_4, S_5, S_7, S_{h1}, S_{h4}) (S_2, S_3, S_5, S_8, S_{h2}, S_{h3}) or (S_2, S_3, S_5, S_8, S_{h1}, S_{h4})
−250	(S_1, S_3, S_5, S_7, S_{h2}, S_{h4}) or (S_2, S_4, S_5, S_7, S_{h1}, S_{h3}) (S_2, S_3, S_5, S_8, S_{h1}, S_{h3})
−300	(S_1, S_3, S_5, S_7, S_{h2}, S_{h3}) or (S_1, S_3, S_5, S_7, S_{h1}, S_{h4})
−350	(S_2, S_3, S_5, S_7, S_{h2}, S_{h4}) or (S_1, S_3, S_5, S_7, S_{h1}, S_{h3})
−400	(S_2, S_3, S_5, S_7, S_{h2}, S_{h3}) or (S_2, S_3, S_5, S_7, S_{h1}, S_{h4})
−450	(S_2, S_3, S_5, S_7, S_{h1}, S_{h3})

The operation of the proposed multilevel converter is described by Fig. 5. Fig. 5(a) shows the configuration of a 15-level proposed multilevel inverter. The carrier and reference signals are shown in Fig. 5(b). The number of carrier signals is obtained by $n_{Carrier} = m - 1 = 14$ [15]. Fig. 5(c) shows the output voltage of V_o. The output voltage frequency spectrum is given in Fig. 5(d). The magnitude of each voltage source in basic structure is considered, $V_1 = V_2 = V_3 = 100$ V and the value of voltage source in H-bridge cell is $V_{H\text{-}bridge} = 50$ V. Table 1 shows ON state switches lookup table for each output voltage level.

3.2. Hybrid asymmetric converter

One disadvantage of topology shown in Fig. 2 is that DC voltage source magnitude cannot be determined as binary and trinary asymmetric states.

In this paper a new method to determine DC voltage magnitudes is proposed based on special sequence, which is taken from Fibonacci series [14]; as follows:

$$\begin{aligned} &\text{for} \quad V_1 = 1pu, \quad V_2 = 1pu \\ &\text{then} \quad V_i = V_{i-1} + V_{i-2}, \quad i = 3, 4, 5, \ldots \end{aligned} \tag{11}$$

Hence, without increase in the number of components, voltage levels increase and waveform being high quality and so structure has been asymmetric. Thus, DC voltage sources value, can be obtained as follows:

$$V_i = \frac{\varphi^i - (1-\varphi)^i}{\sqrt{5}} V_{dc}, \quad i = 1, 2, 3, \ldots, n \tag{12}$$

where n is the number of DC voltage sources and φ is called Golden Ratio that is equal to:

$$\varphi = \frac{1+\sqrt{5}}{2} \tag{13}$$

In asymmetrical proposed topology the number of voltage levels is equal to:

$$m = -\frac{4\sqrt{5}((1-\varphi)^{n+1} - \varphi^{n+1})}{5} - 1 \tag{14}$$

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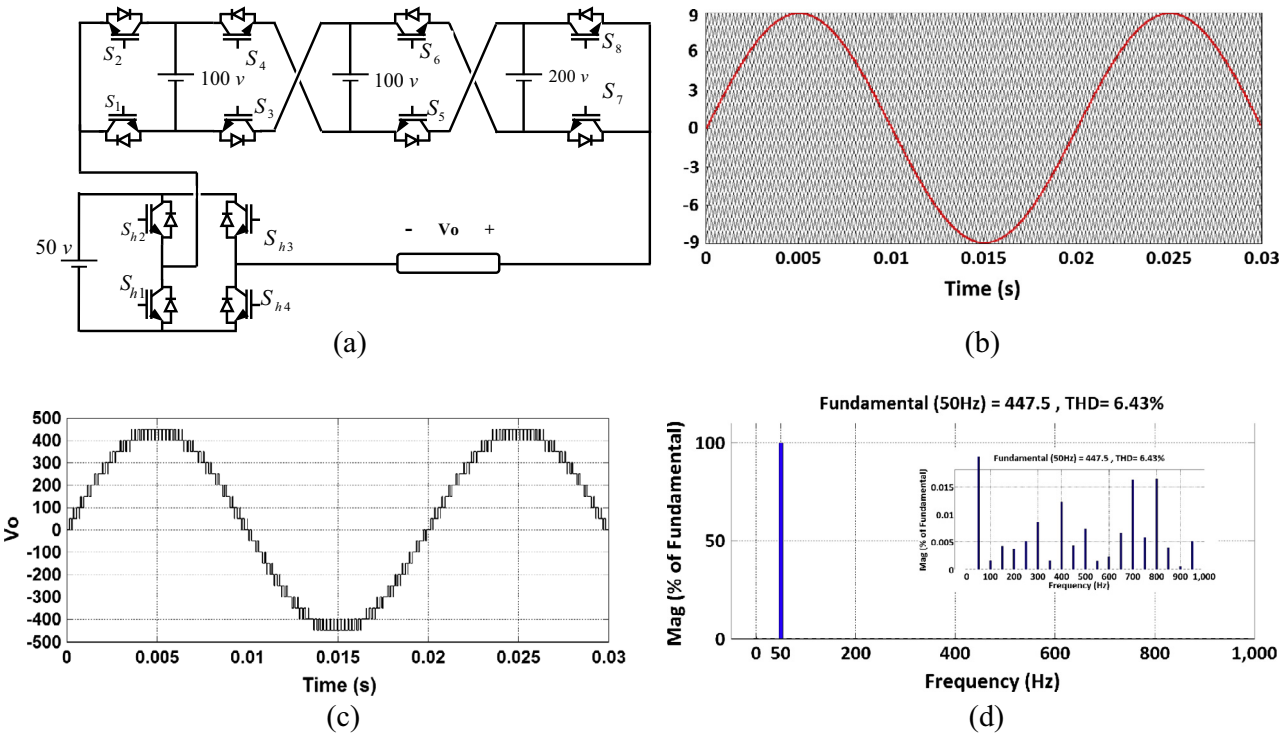

Figure 6 Operation of 19-level proposed asymmetric converter: (a) The configuration of a 19-level proposed asymmetric MLI; (b) Carriers and reference signals; (c) Output voltage; (d) Frequency spectrum of output voltage.

And PIV is obtained by:

$$PIV = \left(2 + 2\frac{\varphi^{n-1} - (1-\varphi)^{n-1}}{\sqrt{5}} + 2\sum_{k=0}^{n-2}\left(\frac{\varphi^{k} - (1-\varphi)^{k}}{\sqrt{5}} + \frac{\varphi^{k+1} - (1-\varphi)^{k+1}}{\sqrt{5}}\right)\right)V_{dc} \quad (15)$$

Thus, value of DC voltage sources in basic structure will be $\{V_{dc}, V_{dc}, 2V_{dc}, 3V_{dc}, 5V_{dc}, 8V_{dc}, 13V_{dc}, \ldots\}$. Fig. 6(a) shows, 19 level hybrid asymmetric proposed topology with $n = 4$ DC voltage sources.

The value of each voltage source in basic structure is considered, {100 V, 100 V, 200 V} and the value of voltage source in H-bridge cell is $V_{H\text{-}bridge} = 50$ V. The carrier and reference signals are shown in Fig. 6(b). The number of carrier signals is $n_{Carrier} = m - 1 = 18$. Output voltage of V_o is presented in Fig. 6(c). Fig. 6(d) shows the output voltage frequency spectrum of the proposed asymmetric topology. Table 2 shows ON state switches lookup table for each output voltage level for asymmetric proposed topology.

Table 3 Number of switches and PIV value for conventional symmetric inverters and proposed.

Symmetric inverter	CMI	Semi cascade	Proposed
m (number of levels)	$2n + 1$	$2n + 1$	$4n - 1$
PIV	$4nV_{dc}$	$(6n - 2)V_{dc}$	$(4n - 2)V_{dc}$
Switches (IGBT)	$4n$	$2n + 2$	$2n + 4$

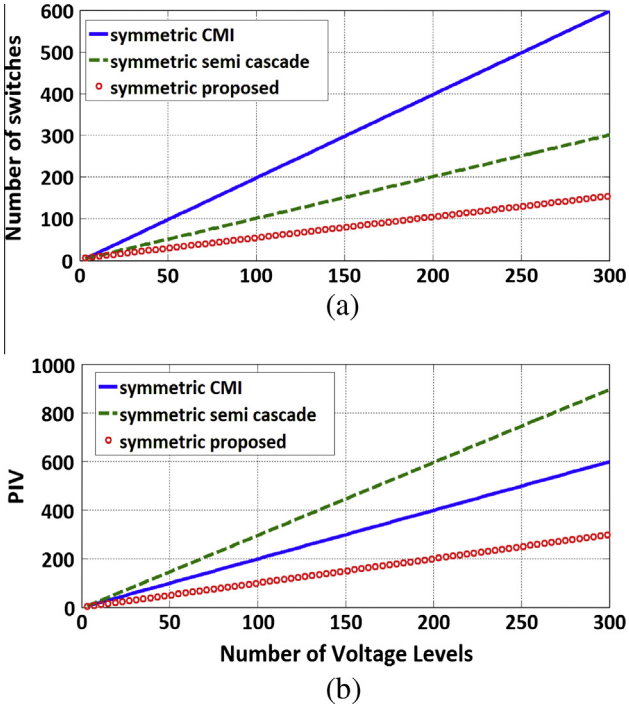

Figure 7 Comparison number of switches and PIV of symmetric topologies: (a) Number of switches; (b) PIV (pu).

Table 4 Number of switches and PIV value for conventional asymmetric inverters and proposed.

Asymmetric inverter	Binary CMI	Trinary CMI	Binary semi cascade	Proposed
m (number of levels)	$2^{n+1}-1$	3^n	$2^{n+1}-1$	$-\frac{4\sqrt{5}((1-\varphi)^{n+1}-\varphi^{n+1})}{5}-1$
PIV	$(2^{n+2}-4)V_{dc}$	$(2\times 3^n-2)V_{dc}$	$(6\times 2^n-6)V_{dc}$	$PIV=\left(2+2\frac{\varphi^{n-1}-(1-\varphi)^{n-1}}{\sqrt{5}}+2\sum_{k=0}^{n-2}\left(\frac{\varphi^k-(1-\varphi)^k}{\sqrt{5}}+\frac{\varphi^{k+1}-(1-\varphi)^{k+1}}{\sqrt{5}}\right)\right)V_{dc}$
Switches (IGBT)	$4n$	$4n$	$2n+4$	$2n+4$

4. Comparison between the proposed multilevel inverter and other topologies

4.1. Symmetric topology

In this section, the proposed topology is compared with other three multilevel inverters. The first comparison index is PIV. The main purpose of this paper, was obtaining least PIV with respect to other topologies of multilevel inverters. In symmetrical hybrid proposed topology, PIV of switches is given by $PIV=(4n-2)V_{dc}$. Table 3, summarizes the number of switches and PIVs for the symmetric cascaded multilevel inverter and symmetric topology of [6] and also proposed symmetric topology respectively, where n is the number of DC voltage sources. As shown in Fig. 7(a), for generate same output levels number, the number of switches for symmetric proposed topology is fewer than other topologies. Also, Fig. 7(b) presents that with the same number of output voltage levels, switches PIV for symmetric proposed topology is fewer.

4.2. Asymmetric topology

Table 4, summarizes the number of switches and PIV for the binary and trinary cascaded multilevel inverter and asymmetric topology of [6] and proposed topology respectively.

Fig. 8 compares number of switches and switches PIV, versus the number of voltage levels, for proposed topology and other asymmetric topologies. As shown in Fig. 8, although the number of switches for synthesizing same number of voltage levels, is further with respect to trinary and binary cascaded multilevel inverter (Fig. 8(a)), but this defect is negligible versus need for least PIV. Switches PIV of proposed asymmetric multilevel inverter, has least value with respect to other topologies. This minimizes total cost of inverter. Comparison PIV is shown in Fig. 8(b).

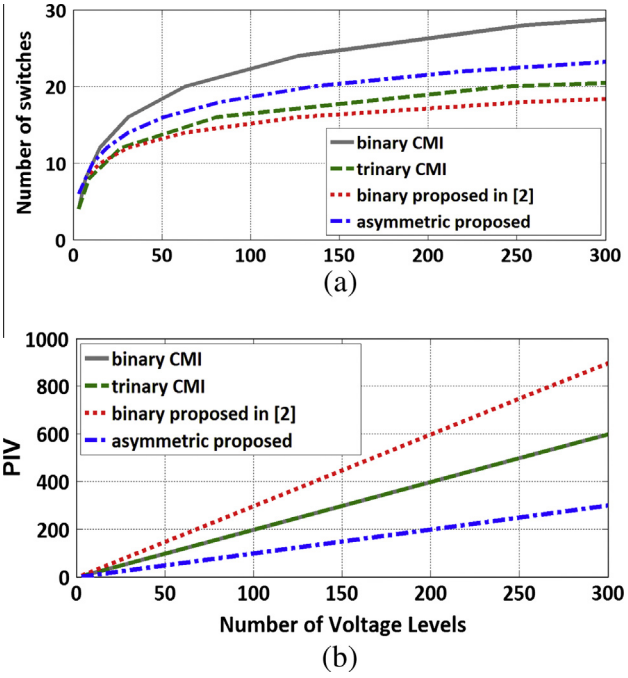

Figure 8 Comparison number of switches and PIV of asymmetric topologies: (a) Number of switches; (b) PIV (pu).

5. Experimental results

In order to validate proposed topology, an experimental prototype of the 19-level asymmetric proposed inverter is implemented. The PCI-1716 DAQ has been used to generate switching pulses. The 74HC573 current buffer has been used to preservation DAQ from high current. The inverter consists of 12 switches power MOSFET-IRFP460 and TLP250 as MOSFET driver. Fig. 9 shows the experimental circuit setup. The parameters of resistive inductive load are 40Ω and $1H$. Carrier waveforms for switching algorithm assumed constant by values of {0.5, 1.5, 2.5, 3.5,...,17.5}. It should be noted that the values of DC voltage sources are {25 V, 50 V, 50 V, 100 V} according to Fibonacci series.

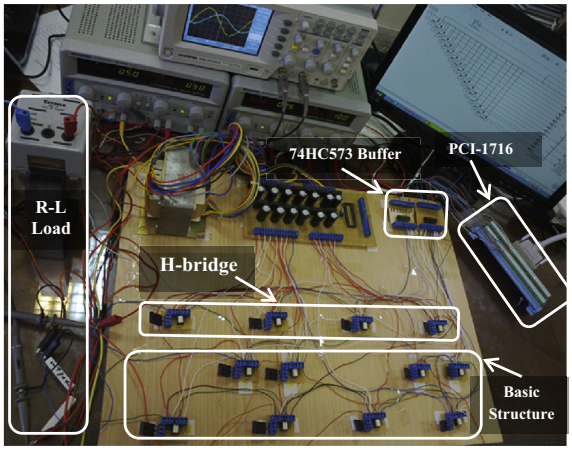

Figure 9 Hardware implementation of 19-level proposed asymmetric multilevel inverter.

Fig. 10(a) depicts experimental waveforms of the voltage and current of load. Fig. 10(b and c) show the output voltage of basic structure (V_B) and H-bridge cell (V_H), respectively. As shown in Fig. 10(a–c), since the four switches H-bridge inverter has been mixed by basic structure as series, the output

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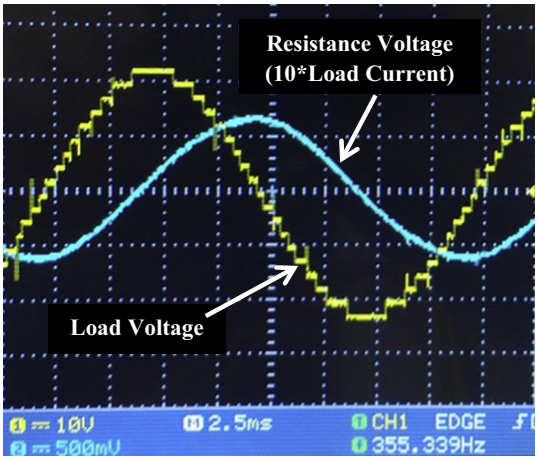
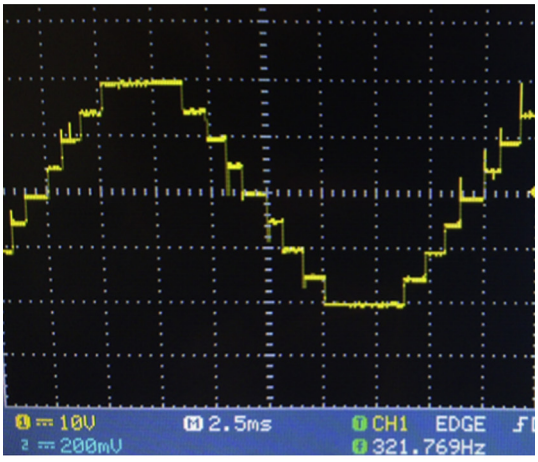
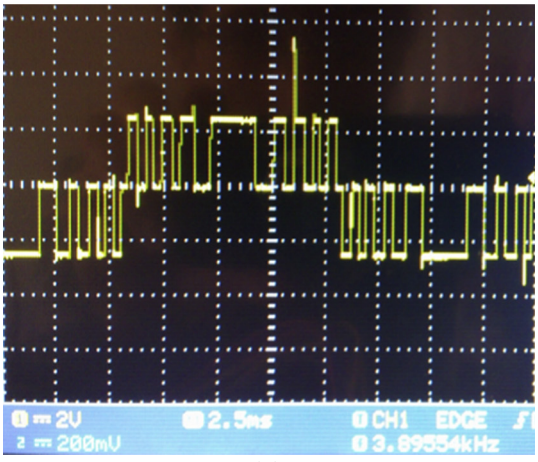


(a)



(b)



(c)

Figure 10 Experimental results: (a) The output voltage ($10 \times 10V/Div$) and resistance voltage (10 * load current) ($10 \times 0.5V/Div$) (b) Output voltage of basic structure, $V_B(10 \times 10V/Div)$; (c) Output voltage of H-bridge cell, $V_H(10 \times 2V/Div)$; (d) Frequency Spectrum.

voltage levels V_O doubled with respect to basic structure voltage. Also the output voltage THD and output current THD are measured respectively 6.79% and 3.34%.

6. Conclusions

In this paper a new topology of symmetric and asymmetric multilevel inverters has been presented. In asymmetric configuration for determination of DC voltage source magnitude, Fibonacci series has been used. This method results in a remarkable reduction in both the PIV and cost of the converter. This is because the selected MOSFETs (or IGBTs) can be of low cost due to low applied voltage with respect to other configurations. Validity of the analysis has been proved by simulation and experimental results.

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